

Analog IC Design Homework 3 (1/7)

● 題目: Fully-differential wide-swing folded-cascode OPAMP

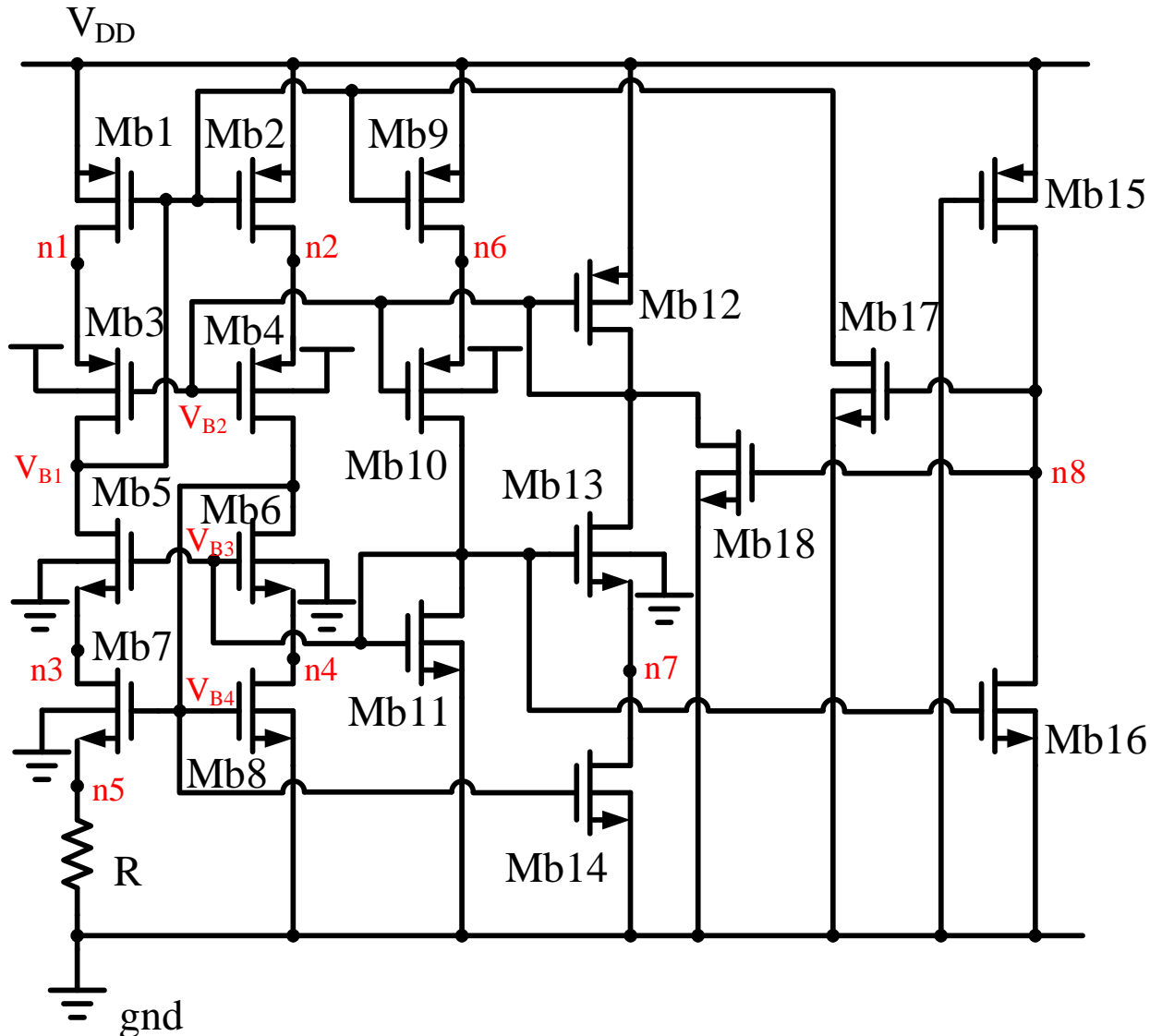
1. 可使用0.18 μm , 16nm 或其他更先進製程 SPICE Model
2. Please size the wide-swing constant- g_m bias circuit with cascode current mirror shown in P.2, the summation of all branch currents should **not exceed 40 μA** with **$V_{\text{eff}_{1\sim6}} > 0.15\text{V}$** and **$V_{\text{eff}_8} > 0.15\text{V}$**
3. Please use the bias circuit designed in 2. and size the Fully-differential wide-swing folded-cascode OPAMP (including common-mode feedback circuit) shown in P.3, the specifications are as follows:
 - ◆ Unity-gain frequency $\geq 200\text{ MHz}$
 - ◆ Phase margin (ϕ_M): $60^\circ \leq \phi_M \leq 66^\circ$
 - ◆ DC gain $\geq 66\text{ dB}$
 - ◆ Slew rate (rise and fall) $\geq 50\text{ V}/\mu\text{s}$ (Use testbench_SR.sp, 10%-90% output level)
 - ◆ Load capacitance (C_L) = 2 pF
 - ◆ Power supply $V_{DD} = 1.8\text{ V}$
(16nm ADFP VDD $\leq 1.05\text{V}$)
4. Please use HSPICE to verify the bias circuit and Fully-differential wide-swing folded-cascode OPAMP
5. Compare and analyze the results between calculation and HSPICE verification

● Note

- ◆ Common-mode feedback circuit should be included and designed in your homework
- ◆ Follow design rules of maximum and minimum transistor width and length
- ◆ Please set the input common mode voltage in a reasonable range
- ◆ External voltage or current sources are not allowed except supply voltage and input common mode voltage (the reference voltage in the common-mode feedback circuit should be generated with voltage divider using resistors)
- ◆ Please use Cadence Virtuoso to build schematic and export the .cir file for verification

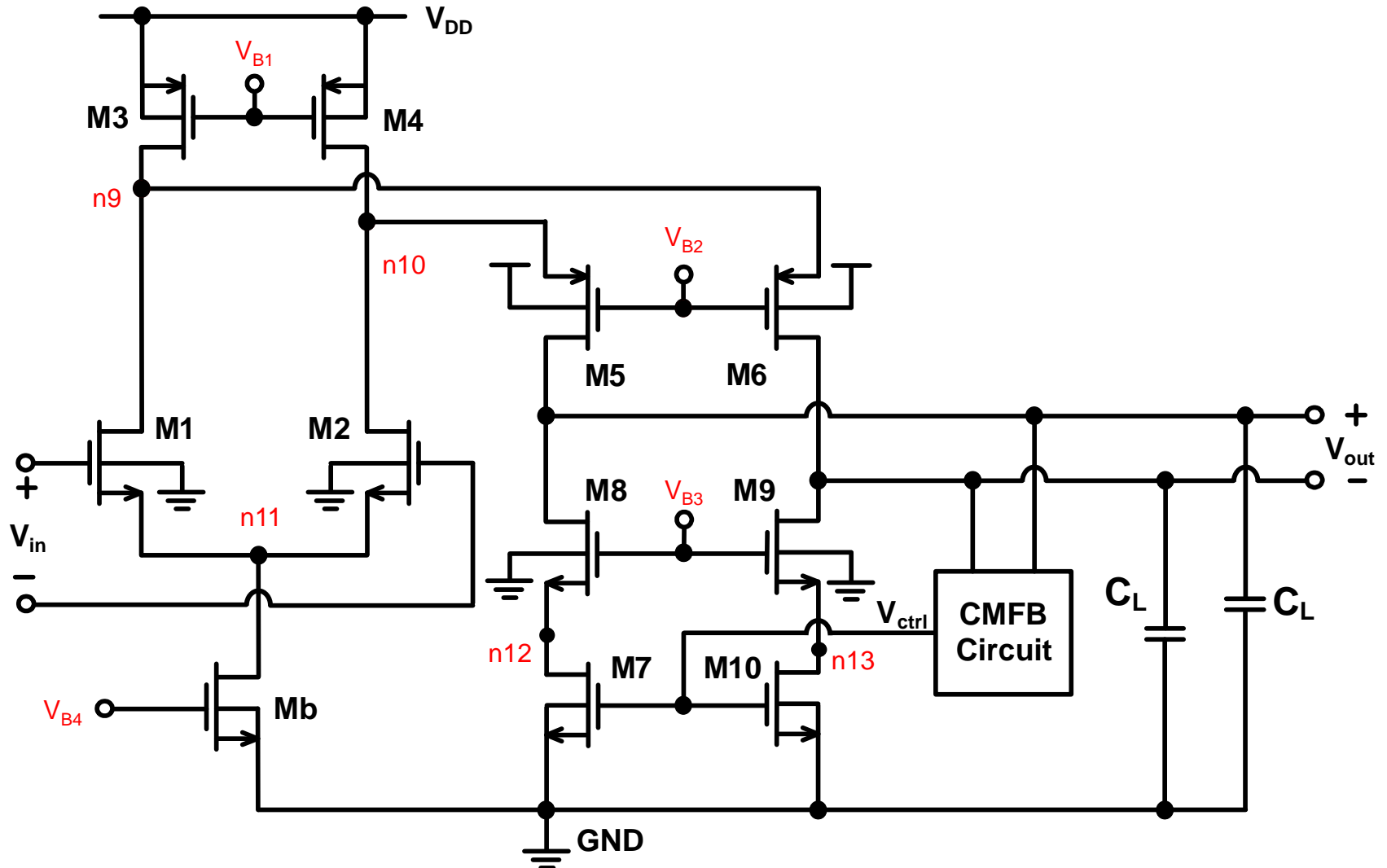
Analog IC Design Homework 3 (2/7)

- Schematic for wide-swing constant-gm bias circuit



Analog IC Design Homework 3 (3/7)

- Schematic for fully-differential wide-swing folded-cascode OPAMP



Analog IC Design Homework 3 (4/7)

- Your report should include
 - ◆ Design flow
 - ◆ HSPICE verification results
 - Nodal voltage and bias current of each transistor. It must be attached to show whether all transistors operate in the appropriate region. (It is recommended to draw the nodal voltages and branch currents directly on the circuit diagram)
 - Please show the Bode plot (including gain and phase) and waveform (slew rate) instead of using “.measure” command in HSPICE to show phase margin or unity gain frequency in the SPICE output text file (because it is easy to be modified).
 - ◆ Virtuoso schematic
 - Include the .cir file and circuit diagram
 - ◆ Calculate the input common mode range and output swing
 - ◆ Area
 - MOSFET : Please calculate the sum of the $W \times L$ for all the MOS used in the designed circuit
$$A_{MOS} = \sum W_i \times L_i$$
 - Capacitor : Just show the capacitance (if used)
 - Resistor : Just show the resistance (if used)
 - ◆ Total current and power consumption
 - ◆ Table of specifications (shown in P.7)
- Note: The total current, power consumption and area should include bias circuits and common-mode feedback circuit.

Analog IC Design Homework 3 (5/7)

● Grading

- ◆ Customization of the .sp file will not be accepted
- ◆ Please name all nodes and transistors as shown in P.2 and P.3
- ◆ Under the condition of achieving all specifications, the smaller power consumption and the smaller area will receive higher scores
- ◆ Please clearly describe the design flow in your report and attach your calculation process, nodal voltage and branch current of each transistor, and V_{eff} results (Please invert color of the attached figure. Please refer to the example in P.6)
- ◆ Report with simulation results only but no design flow will get deducted points according to the situation
- ◆ Report principle: Streamlined and complete content (**Do not copy.**)
 - Report with advanced discussion and analysis will receive higher scores

● Precautions

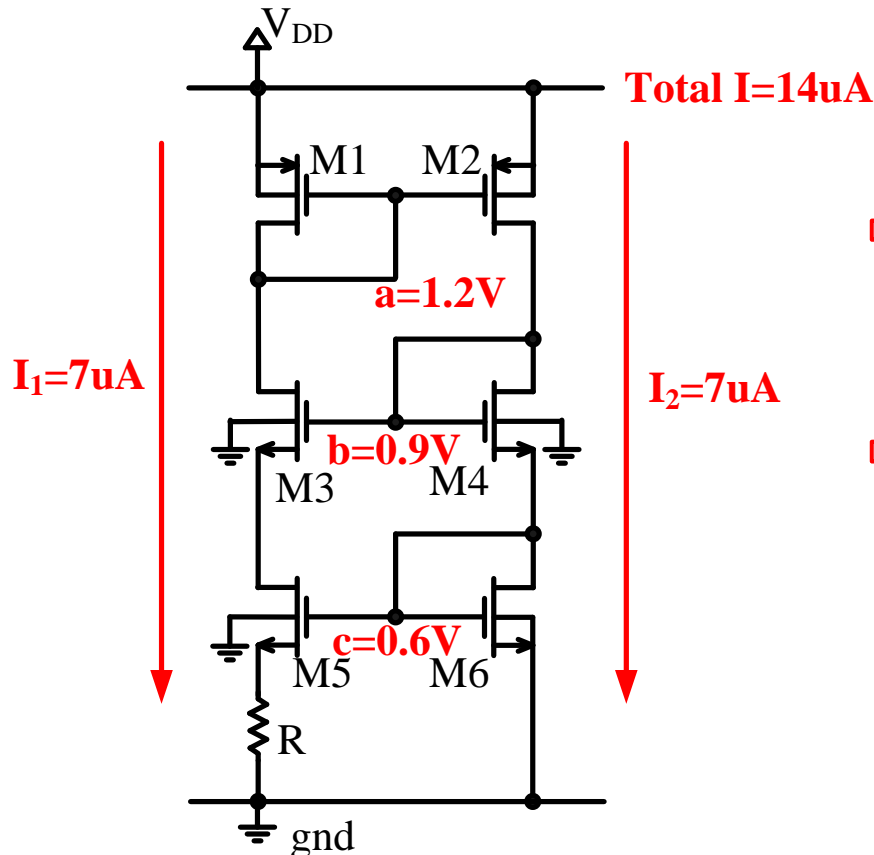
- ◆ Deadline: [11/02/2025\(Sun.\) 23:59:59 pm](#) (不接受作業補交)
- ◆ 使用16nm或更先進製程模擬可自定規格，規格愈佳可獲愈高分
- ◆ Personal work, please upload **Word and HSPICE code (.sp file and .cir file)** to moodle
- ◆ Please compress files into a .zip file and name it as HW#_student ID,
ex: HW2_N26000000 Font size: 12pt (Chinese: 標楷體, English: Times New Roman)
- ◆ Refer to the IEEE submission regulations, set the picture resolution to 300dpi.
- ◆ Upload file size is recommended to be 2MB

Analog IC Design Homework 3 (6/7)

- Example of attached figure (The value of this example is not the result of this homework)
- The transistor number should be consistent with the figure given in the assignment description for easy reading.

◆ Nodal voltage and branch current

◆ V_{eff} results (Available from the .lis file)



element	0:m1	0:m2	0:m3	0:m4	0:m5	0:m6
model	0:p_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-4.3473u	-4.4180u	-4.3473u	-4.4180u	4.3261u	4.4180u
ibs	1.598e-21	1.624e-21	13.9675a	14.6963a	-25.1826a	-24.1428a
ibd	13.9643a	14.6930a	42.2872a	66.1813a	-97.2083a	-60.1641a
vgs	-725.0080m	-725.0080m	-768.2064m	-755.7124m	687.6708m	699.1690m
vds	-239.4341m	-251.9280m	-485.5739m	-882.7238m	796.5523m	398.4067m
vbs	0.	0.	239.4341m	251.9280m	-278.4397m	-266.9415m
vth	-507.7206m	-507.6434m	-569.5798m	-569.7012m	449.3836m	453.1541m
vdsat	-250.2910m	-250.3473m	-240.5100m	-230.5891m	240.1984m	245.8523m
vod	-217.2874m	-217.3646m	-198.6265m	-186.0112m	238.2872m	246.0149m
beta	171.8590u	171.8716u	165.3343u	165.7395u	141.9257u	141.8204u
gam eff	557.0845m	557.0845m	555.4377m	555.3567m	514.7198m	514.4379m
gm	27.8375u	28.6579u	32.4418u	34.7200u	31.1996u	30.4795u
gds	5.9959u	5.3391u	1.9385u	1.2406u	602.9213n	1.2151u
gmb	8.3425u	8.5761u	8.5525u	9.0131u	4.3764u	4.3676u
cdtot	602.2694a	595.6395a	516.0501a	481.1913a	419.0156a	455.6877a
cgtot	637.8033a	636.1121a	626.2839a	624.9136a	961.9485a	965.9698a
cstot	1.0546f	1.0547f	995.4309a	991.7572a	1.2412f	1.2437f
cbtot	1.1033f	1.1010f	974.6619a	938.1662a	891.8941a	923.0924a
cgs	472.5061a	472.3538a	473.5485a	471.8366a	787.5885a	790.1812a
cgd	128.0263a	125.9915a	116.8744a	116.3205a	89.1763a	92.5485a

Analog IC Design Homework 3 (7/7)

- Please attach the following table to the last page of your HW3 report to help TA scoring

Name_ student ID		
DC gain (dB)		
Unit-gain bandwidth (MHz)		
Phase margin		
Slew rate	Rising (V/ μ s)	
	Falling (V/ μ s)	
Input common-mode range		
Output swing		
Area (μm^2)		
Total current (μA)		

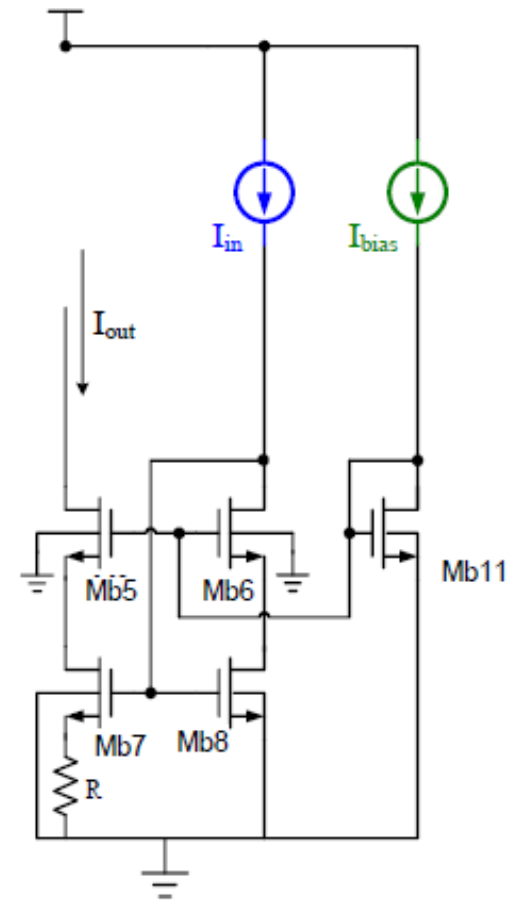
Appendix 1: Design Flow of Bias Circuit

- Step 1: Set $I_{in} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_8 V_{eff8}^\alpha (1 + \lambda V_{DS})$ & $V_{eff8} \rightarrow$ Find $\left(\frac{W}{L}\right)_8$
- Step 2: Set $R \rightarrow$ Use $V_{eff8} = V_{eff7} + I_{out} * R \rightarrow$ Find $\left(\frac{W}{L}\right)_7$
 - ◆ $I_{out} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_7 V_{eff7}^\alpha = I_{in}$
- Step 3: Set V_{eff5} & $V_{eff6} \rightarrow I_5 = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_5 V_{eff5}^\alpha \rightarrow$ Find $\left(\frac{W}{L}\right)_{5,6}$
- Step 4: Set $I_{9,10}$ & $\left(\frac{W}{L}\right)_{11}$ to design V_{B3}

$$V_{B3} - V_{GS6} > V_{eff8}$$

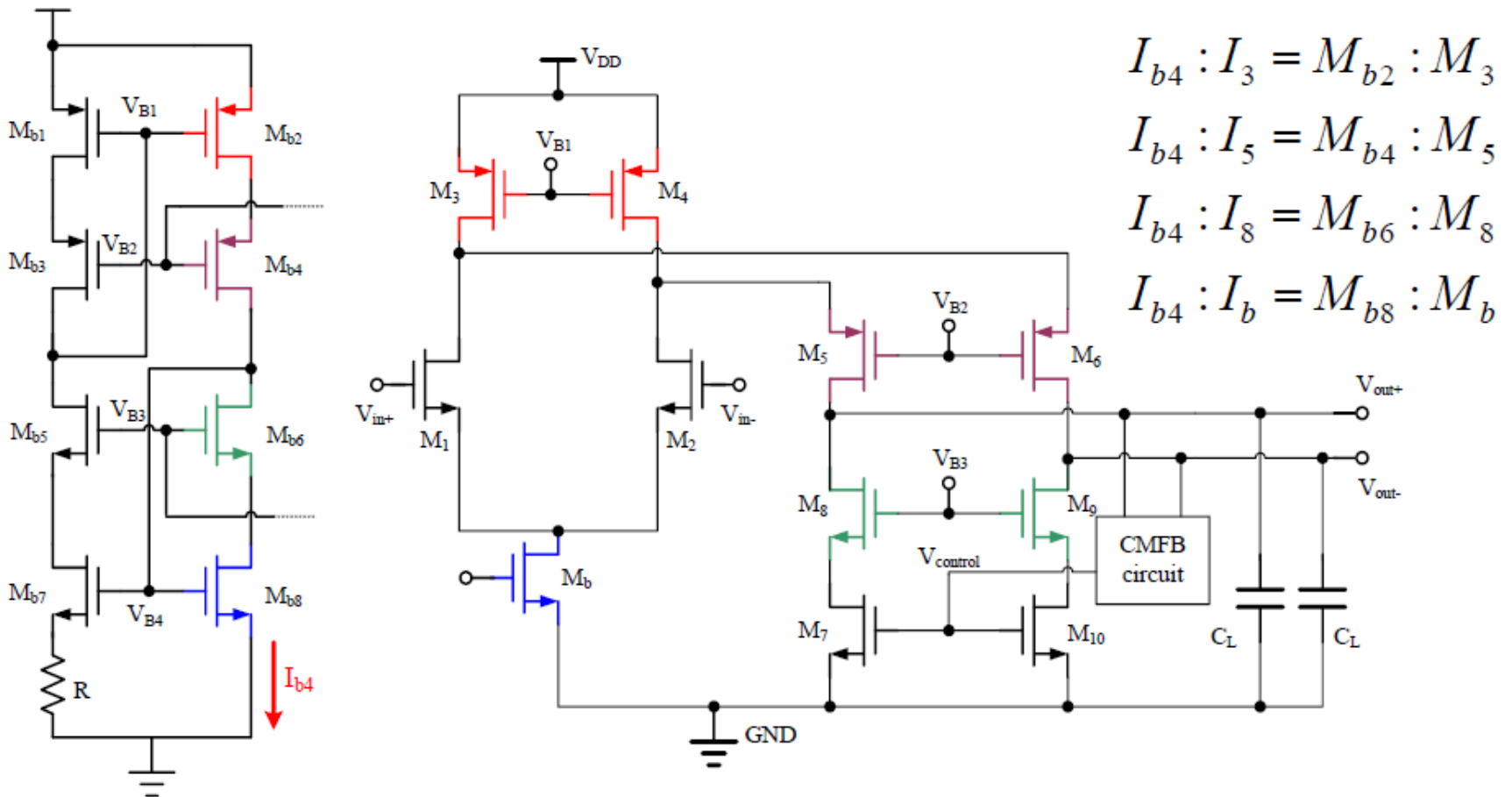
$$V_{GS8} > V_{B3} - V_{t6}$$

- Step 5: Design other transistor size \rightarrow Saturation & V_{eff}
- Step 6: Design start-up circuit



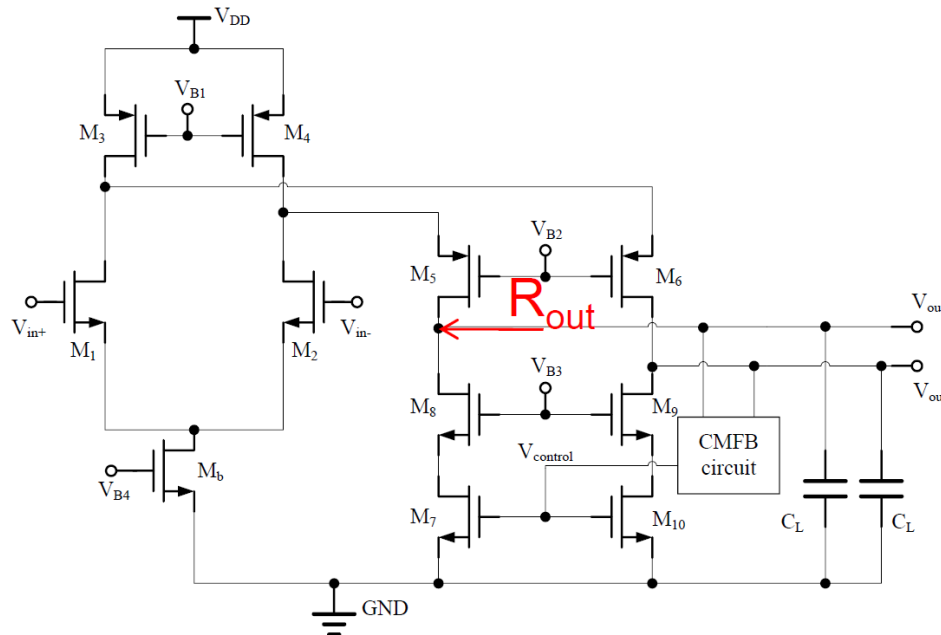
Appendix 2: Design Flow of OPAMP (1/3)

- 假設電流公式 α 為2, 圖NMOS body都接GND、PMOS body都接VDD
- Step 1: M3, M4 (M5, M6, M8, M9) 以及Mb
 - ◆ 由Slew rate 求得 I_3, I_4 以及 I_b ($I_5 = I_3 - I_b/2$)
 - ◆ 利用與 bias circuit 之對應關係求得 M3, M4 (M5, M6, M8, M9) 以及 Mb size



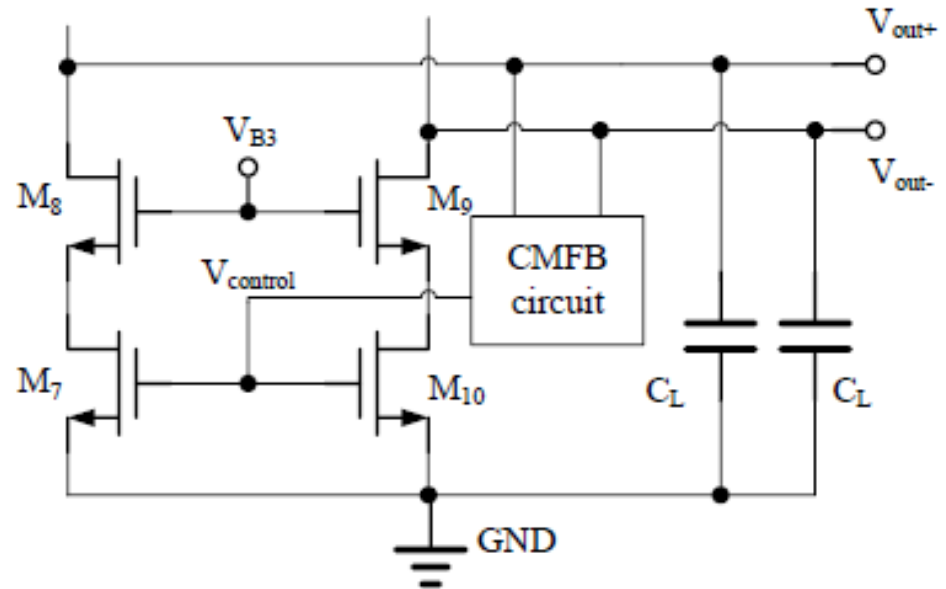
Appendix 2: Design Flow of OPAMP (2/3)

- Step 2: Use $\omega_t = \frac{g_{m2}}{C_L}$, $I_2 = \frac{1}{2}g_{m2}V_{eff2} \rightarrow$ Find M1, M2 size
- Step 3: Find M5, M6, M8, M9 size
 - ◆ $R_{out} = [g_{m5}r_{ds5}(r_{ds2} || r_{ds4})] || [g_{m8}r_{ds8}r_{ds7}]$
 - Assume 所有 V_{eff} 以及 λ 都相同 $\rightarrow R_{out} = \frac{2}{V_{eff} \lambda^2 (I_2 + I_4 + I_7)}$
 - ◆ Gain: $g_{m2}R_{out} = \frac{2g_{m2}}{V_{eff} \lambda^2 (I_2 + I_4 + I_7)} \rightarrow$ Find $V_{eff} \rightarrow$ 利用電流公式求出四顆MOS之W/L



Appendix 2: Design Flow of OPAMP (3/3)

- Step 4: Find M7, M10 size
 - ◆ 設定 V_{out} common mode voltage
 - ◆ 設計 CMFB 得到相對應 $V_{control}$
 - $V_{control} - V_{t10} < V_{B3} - V_{GS9}$
 - ◆ 利用 I_7 (I_{10}) 以及 V_{gs7} (V_{gs10})
 - Find M7, M10 size

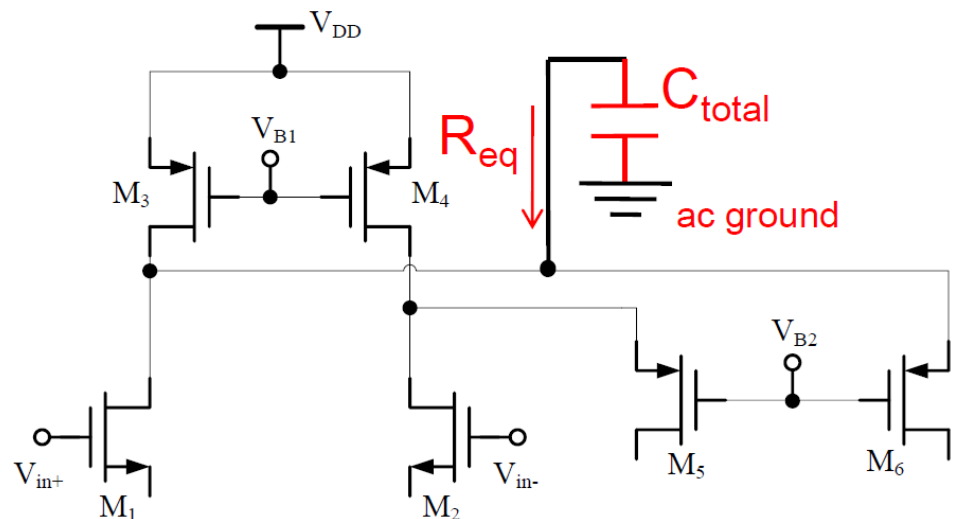


- Step 5: 調整 Phase margin
 - ◆ M5, M6 is PMOS → Smaller g_m

$$w_{p2} \approx \frac{1}{R_{eq} C_{total}}$$

$$R_{eq} = \frac{1}{g_{m6} // r_{ds4} // r_{ds2}}$$

$$C_{total} = C_{gs6} + C_{sb6} + C_{gd3} + C_{db3} + C_{gd1} + C_{db1}$$

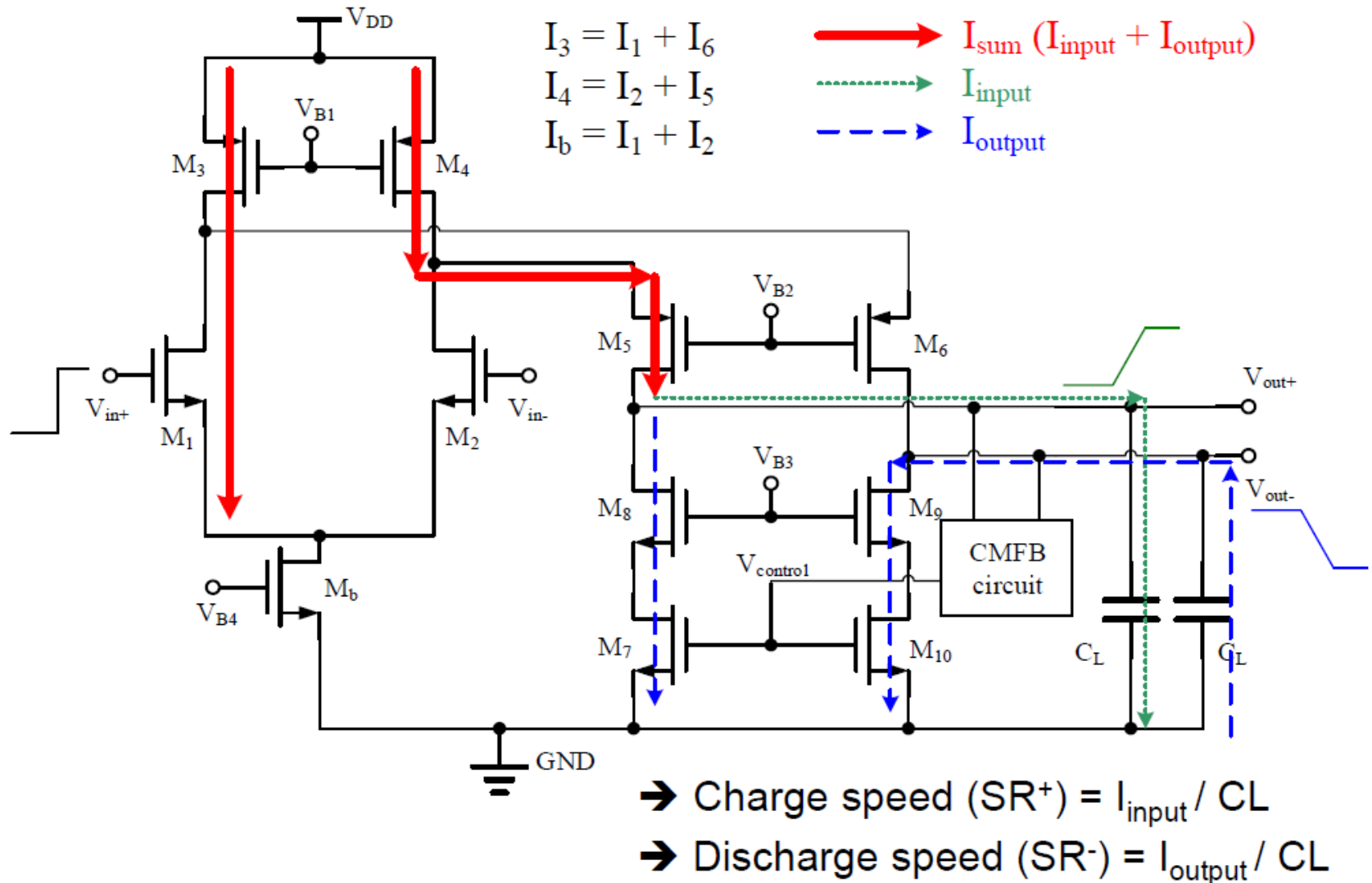


- Circuit operation in steady state



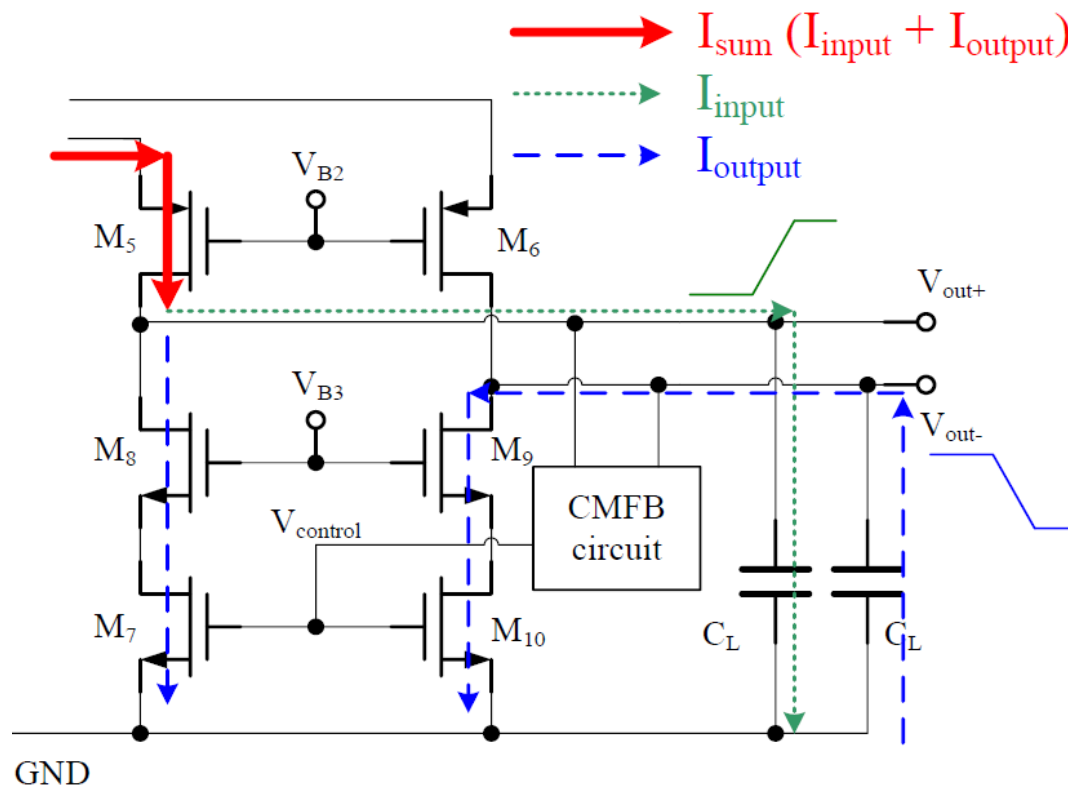
Appendix 3: Slew Rate Consideration (2/4)

- Circuit operation during slewing



Appendix 3: Slew Rate Consideration (3/4)

- $I_{\text{input}} = I_{\text{output}} \rightarrow$ 兩端輸出為differential，CMFB電路不需動作
- $I_{\text{input}} > I_{\text{output}} \rightarrow$ 輸出充電端快，放電端慢 \rightarrow Output common mode voltage $\frac{V_{\text{out}}^+ + V_{\text{out}}^-}{2} \uparrow$
 - ◆ CMFB電路加大 V_{control} \rightarrow 充電端速度變慢，放電端速度加快
- $I_{\text{input}} < I_{\text{output}} \rightarrow$ 輸出放電端快，充電端慢 \rightarrow Output common mode voltage $\frac{V_{\text{out}}^+ + V_{\text{out}}^-}{2} \downarrow$
 - ◆ CMFB電路減小 V_{control} \rightarrow 放電端速度變慢，充電端速度加快



Appendix 3: Slew Rate Consideration (4/4)

- 以上為電路slewing時簡單的運作原理，若更加詳細討論，可發現其中含許多更複雜的因素
- 當 Appendix 3: Slew Rate Consideration (2/4) 情況發生
 - ◆ 流過M5電流由原本的 I_{output} 上升為 I_{sum} → V_{gs5} 上升
 - ◆ M5 source端的電壓也會上升($V_{\text{s5}} = V_{\text{B2}} + V_{\text{gs5}}$)
 - 可能會使M4進入linear region，而經由M4流往M5方向的電流將會小於 I_{sum}
- 當 Appendix 3: Slew Rate Consideration (3/4) 之 $I_{\text{input}} > I_{\text{output}}$ 情況發生
 - ◆ 在CMFB電路加大 V_{control} 時，可能會使M7以及M10進入linear region
 - ◆ 導致 I_7 , I_{10} 電流無法有效上升以維持住output common mode voltage